Abstracts

Low power, high speed PLL fabricated in UTSi/sup (R)/ process

G.C. Wu, D. Kelly, D. Staab and P. Denny. "Low power, high speed PLL fabricated in UTSi/sup (R)/ process." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 165-168.

A CMOS phase locked loop (PLL) design achieves GHz performance, low phase noise, low spurious side-bands and extremely low power (1V, 1GHz, and <1mA of current.) The design is fabricated in 0.5/spl mu/m UTSi/sup (R)/ SOI process which has been previously described [Reedy, 1999].

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